Patent Claims

1. An integrated field-effect transistor (10),

having a substrate region (14) surrounded:

by two terminal regions (16, 18),

by two electrically insulating insulating layers (100, 102), which are arranged at mutually opposite sides of the substrate region (14) and are adjoined by control regions (20, 22),

by at least one electrically insulating region (12, 110),

and by an electrically conductive connecting region (28) or a part (230) of an electrically conductive connecting region between one terminal region (16) and the substrate region (14).

2. The field-effect transistor (10) as claimed in claim 1, wherein the conductive connecting region (28) contains a metal-semiconductor compound or comprises a metal-semiconductor compound, preferably a silicide of a metal having a melting point of greater than 1400 degrees Celsius and/or a refractory metal silicide or a rare earth metal silicide,

and/or wherein the conductive connecting region (230) contains monocrystalline silicon or comprises monocrystalline silicon, the silicon preferably being doped,

and/or wherein the conductive connecting region (230) contains polycrystalline silicon or comprises polycrystalline silicon, the polycrystalline silicon preferably being doped,

and/or wherein the conductive connecting region (28) contains a metal or comprises a metal.

3. The field-effect transistor (10) as claimed in claim 1 or 2, wherein the insulating layers (100, 102) for insulating the control regions (20, 22) from the substrate region (14) have an insulation strength of at least fifteen nanometers or at least twenty nanometers,

and/or wherein the distance between the terminal regions (16, 18) is at least 0.3 micrometer or at least 0.4 micrometer,

and/or wherein one terminal region (16) or both terminal regions (16, 18) have a shallow doping profile gradient which permits a switching voltage having a magnitude of greater than five volts or greater than nine volts or greater than 15 volts, but preferably less than thirty volts or less than 20 volts.

4. The field-effect transistor (10) as claimed in one of the preceding claims, wherein one insulating region (12) is part of an insulating layer which carries a multiplicity of field-effect transistors (10),

and/or wherein the insulating layer contains silicon dioxide or comprises silicon dioxide,

and/or wherein the other insulating region (110) is part of an insulating layer (110), which insulates a multiplicity of substrate regions (14), preferably a silicate glass layer.

5. The field-effect transistor (10) as claimed in one of the preceding claims, wherein the substrate region (14) contains a preferably monocrystalline semiconductor material and/or is doped in accordance with one conduction type, and wherein the terminal

regions (16, 18) are doped in accordance with the other conduction type.

6. The field-effect transistor (10) as claimed in one of the preceding claims, wherein the control regions (20, 22) are electrically conductively connected to one another.

7. The field-effect transistor (10) as claimed in one of the preceding claims, wherein the substrate region (14) contains six side areas, or wherein the substrate region (14) has six side areas,

and/or wherein the terminal regions (16, 18) are arranged at mutually opposite sides of the substrate region (14),

and/or wherein the control regions (20, 22) are arranged at mutually opposite sides of the substrate region (14),

and/or wherein the insulating regions are arranged at mutually opposite sides of the substrate region (14).

8. The use of a field-effect transistor (10) with two control regions (20, 22), in particular a field-effect transistor (10) as claimed in one of the preceding claims,

for switching voltages having a magnitude of greater than five volts or greater than nine volts or greater than fifteen volts, but preferably less than thirty volts.

9. The use of a field-effect transistor with two control regions (20, 22), in particular a field-effect transistor (10) as claimed in one of the preceding claims, as a driving transistor on a word line (372,

388) or a bit line (396) of a memory cell array (330), in particular of a flash memory or of an EEPROM memory,

the driving transistor preferably applying a control voltage to the word line (372, 388) or to the bit line (396).

10. A method for fabricating a field-effect transistor (10), in particular a field-effect transistor (10) as claimed in one of the preceding claims,

having the method steps embodied without restriction by the order specified:

formation of a substrate region (14),

formation of two terminal regions (16, 18) at the substrate region (14),

formation of two electrically insulating insulating layers (100, 102), which are arranged at mutually opposite sides of the substrate region (14) and are adjoined by control regions (20, 22),

and formation of an electrically conductive connecting region (28; 28a, 230), which electrically conductively connects one terminal region (16) and the substrate region (14).

11. The method as claimed in claim 10, wherein the terminal regions (16, 18) and/or the substrate region (14) are/is constructed on the basis of silicon,

and/or wherein the connecting region (28) contains a metal-semiconductor compound, in particular a silicide, or comprises a metal-semiconductor compound, in particular silicide,

and/or wherein the connecting region is produced by means of a self-aligning method in which a metal, in particular a metal having a melting point of greater than 1400 degrees Celsius and/or refractory metal, is deposited, which forms a metal-semiconductor compound at semiconductor regions, in particular a silicide at silicon-based regions,

and/or in which the metal is removed in regions in which metal-semiconductor compound was formed, in particular no silicide.

12. The method as claimed in claim 10 or 11, characterized by the following steps:

provision of an SOI substrate (12),

patterning of the silicon of the SOI substrate, regions remaining in which the substrate region (14) and the terminal regions (16, 18) are intended to be arranged,

formation of the control region (20, 22) after the patterning,

and/or filling of free regions between the regions that remain with an electrically insulating material (30).

13. The method as claimed in one of claims 10 to 12, characterized by the following step:

leveling of the surface, preferably by chemical mechanical polishing, after the filling and/or after the formation of the control regions (20, 22).

14. The method as claimed in claim 13, characterized by the following steps:

etching-back of the control regions after the polishing,

and/or performance of a self-aligning method for forming a metal-semiconductor compound, in particular a salicide method, a metal-semiconductor compound, in particular a silicide layer, being produced in the etched-back regions and/or on the substrate region (14) and/or on a terminal region (16).